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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,120	01/03/2006	Kohichi Morino	R2184.0472/P472	8029

24998 7590 09/03/2008

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
O'TOOLE, COLLEEN J	
ART UNIT	PAPER NUMBER
2816	
MAIL DATE	DELIVERY MODE
09/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/563,120	MORINO ET AL.	
	Examiner	Art Unit	
	COLLEEN O'TOOLE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 2, 2008 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 1 recites the limitation "the differential amplifier circuit" which is connected to the feedback voltage. There is insufficient antecedent basis for this limitation in the claim. It is unclear if the differential amplifier circuit which is connected to the feedback voltage is the differential amplifier circuit in the high-breakdown voltage regulator or the low-breakdown voltage component. For the purposes of examination, "the differential amplifier circuit" has been interpreted as the differential amplifier circuit which is low-

breakdown voltage component. Claims 2-7 are rejected merely for containing the limitations of the parent claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda et al. (U.S. Patent 5,861,771, as recited in the Information Disclosure Statement filed January 3, 2006, hereafter Matsuda) in view of Pulvirenti et al. (U.S. Patent 6,157,176, hereafter Pulvirenti).

Claim 1: Matsuda teaches a semiconductor device (Figure 4) comprising:

a high-breakdown-voltage regulator (circuit generating V_{cc}1 of 7);

a second reference voltage generating circuit (41) structured as a low-breakdown-voltage component (voltage divided V_R) and configured to receive an output voltage (V_R) from the high-breakdown-voltage regulator (output of 7) to generate a reference voltage (V_{REF});

a differential amplifier circuit (51) structured as another low-breakdown-voltage component (voltage divided V_R) and configured to receive the output voltage from the high-breakdown-voltage regulator (output of 7) and the reference voltage (V_{ref}) from the reference voltage generating circuit (41) to produce a drive voltage (V_C);

an output driver (63) structured as a high-breakdown-voltage component (via $V_{CC}1$) and configured to operate based on the drive voltage (V_C), wherein the output driver is a MOS transistor (column 6 lines 45-46); and

resistors (R_3 and R_4) connected in series to the output driver (63) to divide an output voltage of the output driver ($V_{CC}2$) and feed the divided voltage (V_f) back to the differential amplifier circuit (51).

Matsuda does not teach the circuitry which generates voltage VCC1 of 7 in Figure 4. Pulvirenti teaches a voltage regulator (Figure 1) configured to operate at a high input voltage (VBAT), said regulator comprising resistors (R1, R2) connected in series to divide a voltage output (VOUT) from a transistor (M1) connected to a power supply line (VBAT), said transistor (M1) having a gate (G) connected to a differential amplifier circuit (OP1) receiving a first input (+) from a first reference voltage generating circuit (inherent that a circuit generates VBG) and a second input (-) as a feedback voltage divided by said resistors (R1, R2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the voltage regulator taught by Pulvirenti to generate the voltage $V_{CC}1$ taught by Matsuda to optimize the size of the circuit (column 1 lines 19-21). Moreover, the selection of something based on its known suitability for its intended use has been held to support a *prima facie* case of obviousness. *Sinclair & Carroll Co. v. Interchemical Corp.,* 325 U.S. 327, 65 USPQ 297 (1945).

Claim 2: Matsuda further teaches that the high-breakdown-voltage output driver (6) and

the low-breakdown-voltage components (4 and 5) are MOS transistors with gate oxide films having a first thickness (column 2 lines 41-44).

Claim 3: The combined circuit further teaches that the high-breakdown-voltage regulator (Figure 1 of Pulvirenti and Figure 4 of Matsuda) comprises a high-breakdown-voltage MOS transistor with a gate oxide film having a second thickness greater than the first thickness (inherent because the sizes of 4, 5 and 6 are reduced; column 2 lines 41-44).

Claim 4: Matsuda further teaches that the output driver (63; Figure 4) is a P-channel MOS transistor (from Figure 4), the semiconductor device further comprising a diode (11) inserted between the gate and the source of the P-channel MOS transistor (63 of Matsuda) having a reverse breakdown voltage lower than an oxide breakdown voltage of the P-channel MOS transistor (Abstract).

Claim 5: Claim 5 recites the same limitations as claim 4, but using an N-channel MOS transistor. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used an N-channel MOS transistor instead of a P-channel MOS transistor and therefore claim 5 is rejected for the same reasons as claim 4 above. The selection of something based on its known suitability for its intended use has been held to support a *prima facie* case of obviousness. *Sinclair & Carroll Co. v. Interchemical Corp.,* 325 U.S. 327, 65 USPQ 297 (1945).

Claim 7: Matsuda further teaches that the output driver is a P-channel MOS transistor (63; Figure 4), the semiconductor device further comprising a constant current inverter inserted between a power supply line and the output driver, the constant current inverter (6) comprising:

a first N-channel MOS transistor (61) to which the reference voltage (Vref) generated by the reference voltage generator is supplied (via 51);

a first P-channel MOS transistor (62) connected in series to the first N-channel MOS transistor (61) to produce a constant current (mirrors current from 61);

a second P-channel MOS transistor (63) defining a constant current circuit under a current mirror configuration (mirrors current from 62); and

Matsuda does not explicitly teach a second N-channel MOS transistor to which the drive voltage output from the differential amplifier circuit is supplied. However, it is known in the art to use self-biased MOS transistors to be resistive components R3 and R4. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a second N-channel MOS transistor to drive the voltage output from the differential amplifier for resistor R3. The selection of something based on its known suitability for its intended use has been held to support a *prima facie* case of obviousness. *Sinclair & Carroll Co. v. Interchemical Corp.,* 325 U.S. 327, 65 USPQ 297 (1945).

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda in view of Pulvirenti, and further in view of Iravani (U.S. Patent 5,936,460).

Claim 6: Matsuda further teaches that the output driver (63; Figure 4) is a P-channel MOS transistor (as seen in Figure 4). Neither Matsuda nor Pulvirenti teach a constant current inverter circuit. Iravani teaches constant current circuit (Figure 2) inserted between the differential amplifier circuit ($V_{CC}1$ of Matsuda) and the output driver (63 of Matsuda), the constant current inverter comprising:

a constant current circuit (Iref2) connected between a power supply line (Vdd) and the output driver (63 of Matsuda); and

a MOS transistor (61 of Matsuda) controlled by the drive voltage output (V_C of Matsuda) from the differential amplifier circuit (51 of Matsuda).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the current source taught by Iravani in the regulator circuit taught by Matsuda to provide a stable, noise-free output current (column 1 lines 16-18, column 3 lines 58-59 of Iravani, where the internal circuits of Matsuda require high precision; column 3 lines 16-21).

Claims 8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda in view of Iravani, further in view of Negoro et al. (JP2002270781A as recited on the Information Disclosure Statement filed January 3, 2006, hereafter Negoro), and further in view of Pulvirenti.

Claim 8: Matsuda teaches a semiconductor device (Figure 4) comprising:

a reference voltage generating circuit (41) configured to generate a reference voltage (Vref);

a differential amplifier circuit (51) configured to receive the reference voltage (Vref) and generates a drive voltage (Vc);

an output driver (63) configured to operate based on the drive voltage (Vc), wherein the output driver is a MOS transistor (column 6 lines 45-46);

resistors (R3 and R4) connected in series to the output driver (63) to divide an output voltage (Vcc2) of the output driver (63) and feed the divided voltage (Vf) back to the differential amplifier circuit (51).

Matsuda does not teach a constant current circuit. Iravani teaches a constant current circuit (Figure 2) inserted between a power supply line (Vdd) and a combination of the reference voltage generating circuit (Iref1 connected to Vref of Matsuda) and the differential amplifier circuit (Iref2 connected to 61 of Matsuda). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the current source taught by Iravani in the regulator circuit taught by Matsuda to provide a stable, noise-free output current (column 3 lines 58-59).

Neither Matsuda nor Iravani teach a diode having a reverse breakdown voltage lower than an oxide breakdown voltage of the MOS transistor. Negoro teaches a diode (11; Figure 1) inserted between a gate and a source of the MOS transistor (5 corresponding to 63 of Matsuda), the diode (11) having a reverse breakdown voltage lower than an oxide breakdown voltage of the MOS transistor (Abstract, where the reverse breakdown of the protective diode is about half the gate-oxide-film breakdown

voltage of the transistor 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the diode taught by Negoro in the combined circuit taught by Matsuda and Iravani to prevent damage to the gate oxide film of a transistor (Abstract).

Neither Matsuda, Iravani, nor Negoro teach the inherent circuit which generates voltage VCC1 of 7 in Figure 4. Pulvirenti teaches a voltage regulator (Figure 1) configured to operate at a high input voltage (VBAT), said regulator comprising resistors (R1, R2) connected in series to divide a voltage output (VOUT) from a transistor (M1) connected to a power supply line (VBAT), said transistor (M1) having a gate (G) connected to a differential amplifier circuit (OP1) receiving a first input (+) from a first reference voltage generating circuit (inherent that a circuit generates VBG) and a second input (-) as a feedback voltage divided by said resistors (R1, R2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the voltage regulator taught by Pulvirenti to generate the voltage $V_{CC}1$ taught by Matsuda to optimize the size of the circuit (column 1 lines 19-21). Moreover, the selection of something based on its known suitability for its intended use has been held to support a *prima facie* case of obviousness. *Sinclair & Carroll Co. v. Interchemical Corp.,* 325 U.S. 327, 65 USPQ 297 (1945).

Claim 11: Iravani further teaches that the constant current circuit (Figure 2) includes multiple MOS transistors connected in series to form a multi-stage constant current circuit (61 of Matsuda is in series with m1 of Iravani).

8. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda, Iravani, Negoro and Pulvirenti as applied to claim 8 above, and further in view of Menegoli et al. (U.S. Patent Application Publication 2004/0046532, hereafter Menegoli). Matsuda, Iravani, and Negoro teach the circuit as recited in claim 8 above. Neither Matsuda, Iravani, nor Negoro teaches that the constant current circuit (7; Figure 6) is structured by depression-mode or enhancement mode NMOS or PMOS transistor. Menegoli teaches that MOSFET transistors can be made either enhancement or depletion by adjusting the surface concentration of the channel region. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used enhancement or depletion mode NMOS or PMOS transistors to adjust the threshold of the NMOS or PMOS transistors ([0020]).

Response to Arguments

9. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to COLLEEN O'TOOLE whose telephone number is (571)270-1273. The examiner can normally be reached on M-F 8:30-5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/QUAN TRA/
Primary Examiner, Art Unit 2816

/C. O./
Examiner, Art Unit 2816